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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
UMEZ ERONINI, LYNETTE T	

ART UNIT	PAPER NUMBER
1765	

MAIL DATE	DELIVERY MODE
08/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,188	EMA ET AL.	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5 and 19-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *2,5 and 24-27* is/are allowed.

6)☒ Claim(s) *1,3 and 19-23, and 28* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/11/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 3, 19-23, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poon (US 5,328,533) in view Minami (US 4,252,840).

Poon teaches a method for fabricating a semiconductor device comprising the steps of:

forming a conductor pattern **51** over a semiconductor substrate **50** (column 5, lines 27-39);

forming a first insulation film **34** covering the conductor pattern (column 5, lines 41-43);

forming over the first insulation **34** film a second insulation **36** film (column 5, lines 45-53);

forming over the second insulation film **36** a third insulation film **38** (column 5, lines 61-64); and

forming a hole **18** in the third insulation film **10**, the second insulation film **13** and the first insulation film **15** (column 6, lines 3-24), **in claim 1**; and

further comprising steps of forming capacitors, bitlines and wiring layers to constitute a memory device (column 5, lines 33-38), **in claim 23**.

Poon teaches an embodiment in which dielectric layers **34**, **36**, and **38** above are similar to interlevel dielectric layers **16**a, **16**b, and **16**c (same as Applicants' first, second, and third dielectric layers respectively), which are formed over a substrate, and wherein **16**a and **16**c can be made of silicate glass material and **16**b can be a polish stop layer and made of silicon nitride (column 3, lines 48-57). Hence, the aforementioned reads on, forming over the first insulation layer a second insulation film having etching characteristics different from those of the first insulation film; and

forming over the second insulation film a third insulation film having etching characteristics different from those of the second insulation film, **in claim 1**; and

in the first step, the insulation film is etched with the second insulation film as a stopper, **in claim 19;**

wherein the first insulation film and the third insulation film comprises silicon oxide, **in claim 20 and 22**; and

wherein the second insulation film comprises silicon nitride, **in claim 21**.

Poon differs in failing to teach

the step of forming the hole including a first step of etching the third insulation, a second step of etching the second insulation film, and a third step of etching the first insulation film; an etching condition at the first step being different form that at the second step, **in claim 1**;

in the third step, the opening is opened down to semiconductor substrate (column 6, lines 22-24), **in claim 3**.

the step of forming the hole including a first step of etching the third insulation film, a second step or etching the second insulation film and a third step of etching the first insulating film, an etching condition at the first step being different from that at the second step; and

wherein in the step of forming the hole, an etching rate of the second insulation film at the first step is lower than an etching rate of the third insulation film at the first step and an etching rate of the second insulation film at the second step, **in claim 28**.

Minami teaches first, second and third insulating layers **7, 10, and 11** are made of different materials and etched at different rates (column 2, line 55 - column 3, line 10 and 20-22). The aforementioned also reads on a second insulation film having etching characteristics different from those of the first insulation film and a second insulation film a third insulation film having etching characteristics different from those of the second insulation film and an etching condition at the first step being different form that at the second step, **in claim 1**. Further, Minami's method of etching suggests each insulating

layer is etched individually, therefore, Minami's etching method reads on, wherein in the step of forming the hole, an etching rate of the second insulation film at the first step is lower than an etching rate of the third insulation film at the first step and an etching rate of the second insulation film at the second step, **in claim 28**.

Hence, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Poon by using Minami's method of etching insulating layers because such method is used in a method of manufacturing semiconductor device with good yield and in the highly integrated form (Minami, column 1, lines 33-35).

Allowable Subject Matter

4. Claims 2, 5, and 24-27 are allowed.

5. The following is an examiner's statement of reasons for allowance:

As to claims 2, 5, and 24-27, the prior art of record taken alone or in combination fails to suggest, teach or render obvious a method for fabricating the semiconductor device, as defined the steps of the claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicants did not present arguments in Remarks filed 5/4/2007 and 5/18/2007 with respect to the rejection of claims 1, 3, 4, and 15 and 19 under 35 U.S.C 103(a) over Shono et al. (US 5,365,095) in view of Minami (US 4,222,840);

However, Applicants' amendment filed in 5/4/2007 with respect to claim 1 has been considered but are moot in view of the new ground(s) of rejection because the formerly applied references failed to teach "wherein in the third step of etching the first insulation film, the opening is opened down to the conductor pattern" as recited in (Currently Amended) Claim 1. Hence, a new art rejection has been made to address the third step of etching the first insulation film, the opening is opened down to the conductor pattern.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 1765

ltue

August 14, 2007

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER